REMARKS

In Item 3 of the Office Action of December 1, 2004, the disclosure was objected to because of various informalities on page 34. The text of page 34 is amended herewith to overcome these objections.

In Item 4 of the Office Action, claims 1 and 5-8 were rejected under 35 U.S.C. 102(b) as being anticipated by Pilo (US 5,343,428). Claim 1 is directed to:

> 1. A sense amplifier, comprising:
> a sampling circuit receiving an input signal to the sense amplifier;
> a reference node operable to store a reference signal corresponding to the input data; and
> a timing circuit activating the sampling circuit a predetermined interval before measurement of the input signal is to be taken, the sampling circuit admitting the input signal to the reference node thereby.

The Examiner asserts that the "reference node" of claim 1 reads on node 101 or 102 of Pilo. Applicant respectfully disagrees. Nodes 101 and 102 of Pilo are not reference nodes of the differential amplifier 25, operable to store a reference signal. Similarly, the "sampling circuit" of Pilo does not admit the input signal (MUXLAT or MUXLAT*) to a reference node. Therefore, Applicant submits that claim 1 is not anticipated by Pilo.

Additionally, the "timing circuit" of Pilo does not activate the "sampling circuit" a predetermined interval before measurement of the input signal is to be taken, as called for in claim 1. Rather, the "timing circuit" merely activates the taking of said measurement when the measurement is to be taken. Referring to FIG. 2 and column7, lines 51-60 of Pilo, the transition of the CLK signal from low to high at time t4 causes the transfer gates 43 and 52 (the "sampling circuit") to become conductive and the input signals MUXLAT and MUXLAT* are allowed to propagate through the BICMOS sense amplifier 20, as indicated by the successive transitions of the voltage levels of node 101, node 102, node 103, node 104 and output signals PED and PED* after time t4. The Examiner asserts that "the input signal MUXLAT* is provided to node 102 prior to the sense amplifier comparison." Applicant disagrees. Rather it is the transition of the

CLK signal from low to high that causes the input signals MUXLAT and MUXLAT* to be admitted to the differential amplifier 25, as indicated by the transitions of the voltage levels of node 101, node 102, node 103, node 104 and output signals PED and PED* after time t4. The Examiner also asserts that the sense amplifier of Pilo is enabled by signal OE. Again, Applicant respectfully disagrees. The OE signal merely causes the differential voltages on nodes 101 and 102, nodes 103 and 104, and data output signals PED and PED* to be reduced, thus providing for low power consumption (see column 7, lines 41-50). The input signals MUXLAT and MUXLAT* are not provided to the differential amplifier 25 of Pilo until the CLK transitions from low to high at time t4. Thus, Applicant submits that claim 1 is not anticipated by Pilo.

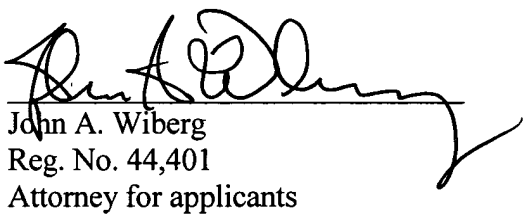
Claim 5 is similar to claim 1 and was rejected under the same grounds as claim 1. Therefore, Applicant submits that claim 5, and claims 6-8 depending therefrom, are not anticipated by Pilo for at least the reasons set forth above with respect to claim 1.

In view of the foregoing, Applicant respectfully requests reconsideration and allowance of claims 1 and 5-8.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Date: March 1, 2005

Respectfully submitted,



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